

BUK6Q12-40P

40 V, P-channel Trench MOSFET

15 May 2025

Product data sheet

1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in an MLPAK33 (SOT8002-3) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Logic-level compatible
- Trench MOSFET technology
- Side-wettable flanks for optical solder inspection
- Thermally efficient package in a small form factor (3.3 mm x 3.3 mm footprint)
- AEC-Q101 qualified

3. Applications

- Reverse polarity protection
- High-speed line driver
- High-side load switch
- Relay driver

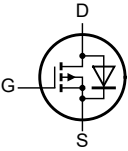
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_J \leq 175\text{ °C}$	-	-	-40	V
V_{GS}	gate-source voltage	$T_J = 25\text{ °C}$	-20	-	20	V
I_D	drain current	$V_{GS} = -10\text{ V}; T_{mb} = 25\text{ °C}$	-	-	-64	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$	-	-	94	W
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = -10\text{ V}; I_D = -9.1\text{ A}; T_J = 25\text{ °C}$	-	9.9	12.4	mΩ

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 MLPAK33 (SOT8002-3)	 017aaa094
2	S	source		
3	S	source		
4	G	gate		
5	D	drain		
6	D	drain		
7	D	drain		
8	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK6Q12-40P	MLPAK33	plastic thermal enhanced surface mounted package with side-wettable flanks (SWF); mini leads; 8 terminals;pitch 0.65 mm; 3.3 x 3.3 x 0.8 mm body	SOT8002-3

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK6Q12-40P	NXC

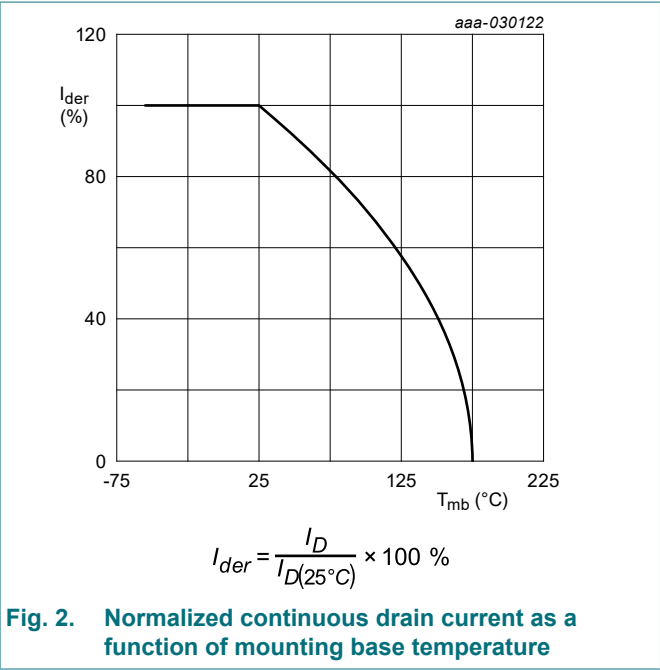
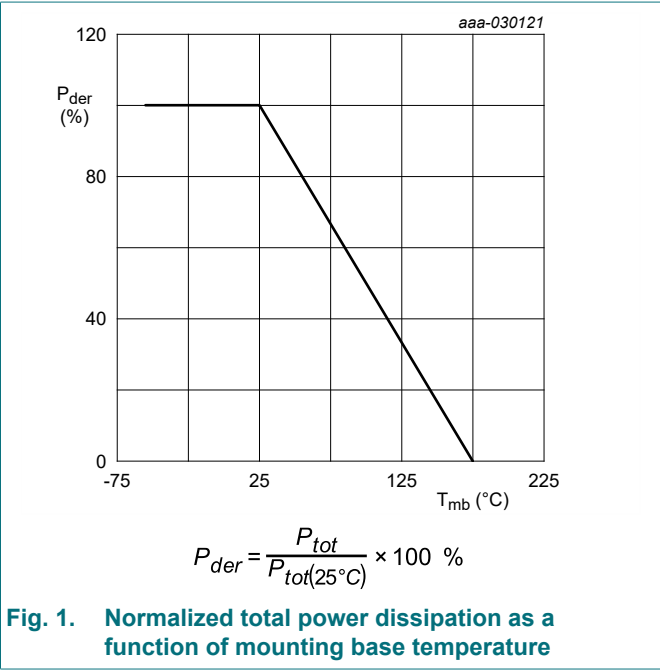
8. Limiting values

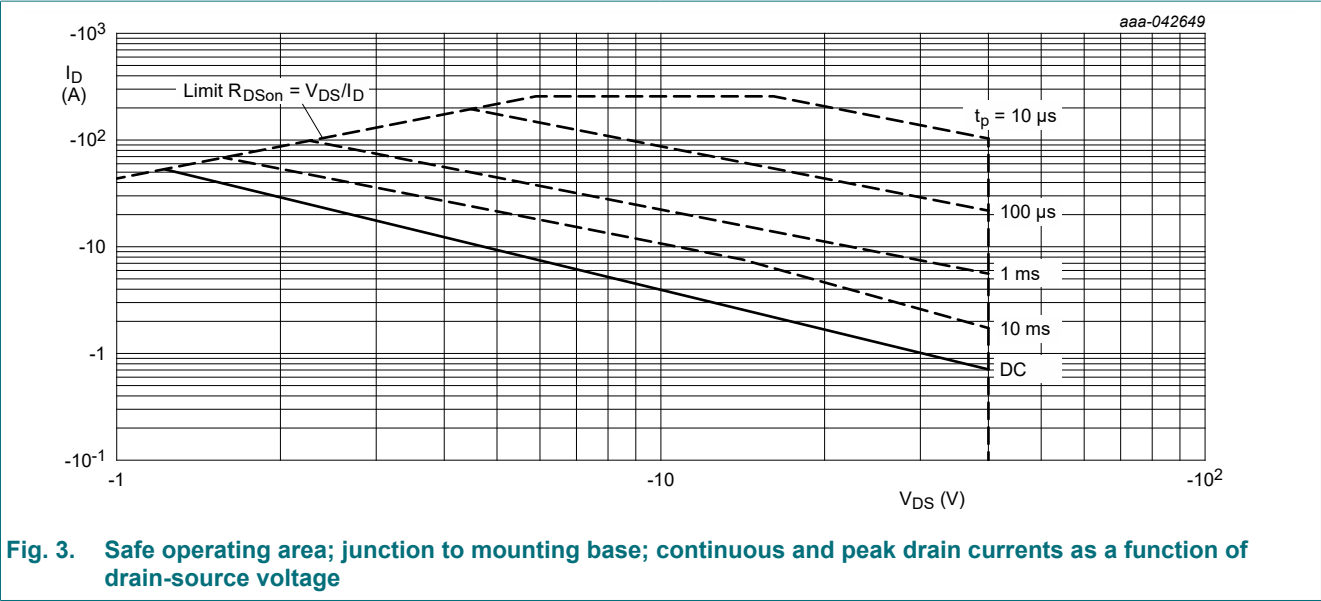
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C		-	-40	V
V _{GS}	gate-source voltage	T _j = 25 °C		-20	20	V
I _D	drain current	V _{GS} = -10 V; T _{mb} = 25 °C		-	-64	A
		V _{GS} = -10 V; T _{mb} = 100 °C		-	-45	A
I _{DM}	peak drain current	T _{mb} = 25 °C; single pulse; t _p ≤ 10 μs		-	-256	A
P _{tot}	total power dissipation	T _{mb} = 25 °C		-	94	W
T _j	junction temperature			-55	175	°C
T _{amb}	ambient temperature			-55	175	°C
T _{stg}	storage temperature			-65	175	°C
Source-drain diode						
I _S	source current	T _{mb} = 25 °C		-	-64	A
I _{SM}	peak source current	T _{mb} = 25 °C; single pulse; t _p ≤ 10 μs		-	-256	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V _{sup} ≤ -40 V; V _{GS} = -10 V; T _{j(init)} = 25 °C; R _{GS} = 50 Ω; I _D = -39.5 A; unclamped	[1] [2]	-	136	mJ
I _{AS}	non-repetitive avalanche current	T _{j(init)} = 25 °C	[3]	-	-39.5	A

- [1] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
[2] Refer to application note AN10273 for further information.
[3] Protected by 100% test.





9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	60	80	K/W
$R_{th(j-mb)}$	thermal resistance from junction to mounting base			-	1	1.6	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm².

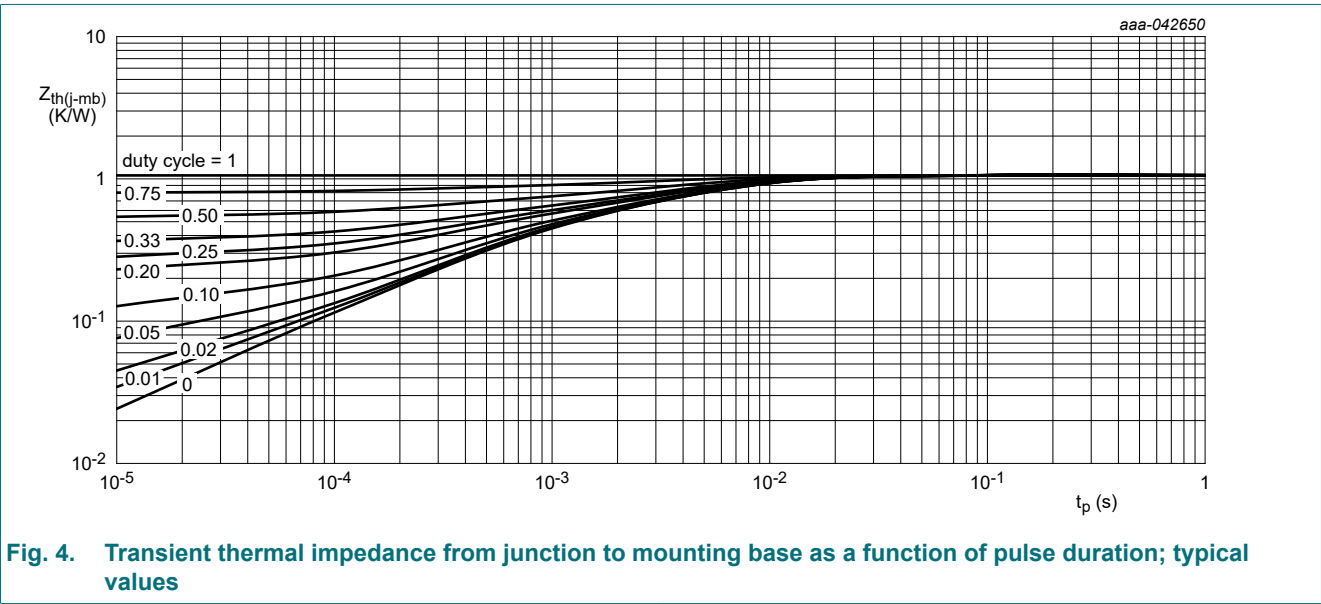


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = -250 μA; V _{GS} = 0 V; T _j = 25 °C		-40	-	-	V
V _{GSth}	gate-source threshold voltage	I _D = -1 mA; V _{DS} = V _{GS} ; T _j = 25 °C		-1.4	-2	-2.7	V
I _{DSS}	drain leakage current	V _{DS} = -40 V; V _{GS} = 0 V; T _j = 25 °C		-	-	-1	μA
I _{GSS}	gate leakage current	V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C		-	-	-100	nA
		V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C		-	-	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = -10 V; I _D = -9.1 A; T _j = 25 °C		-	9.9	12.4	mΩ
		V _{GS} = -10 V; I _D = -9.1 A; T _j = 175 °C		-	18	23	mΩ
		V _{GS} = -4.5 V; I _D = -6.5 A; T _j = 25 °C		-	15.9	24.5	mΩ
g _{fs}	forward transconductance	V _{DS} = -5 V; I _D = -9.1 A; T _j = 25 °C		-	26.6	-	S
R _G	gate resistance	f = 1 MHz		-	6	-	Ω
Dynamic characteristics							
Q _{G(tot)}	total gate charge	V _{DS} = -20 V; I _D = -9.1 A; V _{GS} = -10 V; T _j = 25 °C		-	72	108	nC
Q _{GS}	gate-source charge			-	12	-	nC
Q _{GD}	gate-drain charge			-	16	-	nC
C _{iss}	input capacitance	V _{DS} = -20 V; f = 1 MHz; V _{GS} = 0 V; T _j = 25 °C		-	3800	-	pF
C _{oss}	output capacitance			-	290	-	pF
C _{rss}	reverse transfer capacitance			-	250	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = -20 V; I _D = -9.1 A; V _{GS} = -10 V; R _{G(ext)} = 5 Ω; T _j = 25 °C		-	6	-	ns
t _r	rise time			-	15	-	ns
t _{d(off)}	turn-off delay time			-	91	-	ns
t _f	fall time			-	33	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = -1.9 A; V _{GS} = 0 V; T _j = 25 °C		-	-0.7	-1.2	V
t _{rr}	reverse recovery time	I _S = -1.9 A; dI _S /dt = 100 A/μs; V _{GS} = 0 V; V _{DS} = -20 V; T _j = 25 °C		-	20	-	ns
Q _r	recovered charge			-	14	-	nC

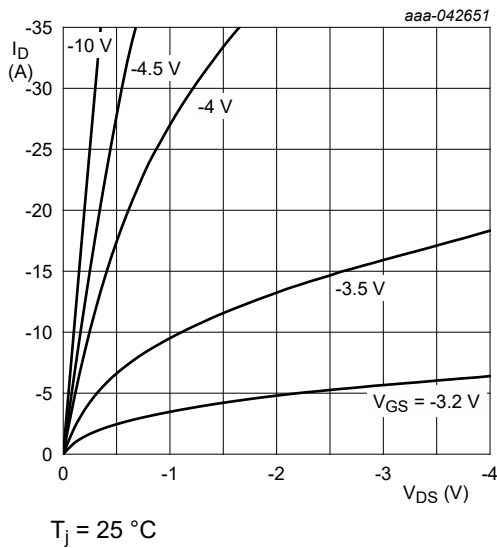


Fig. 5. Output characteristics: drain current as a function of drain-source voltage; typical values

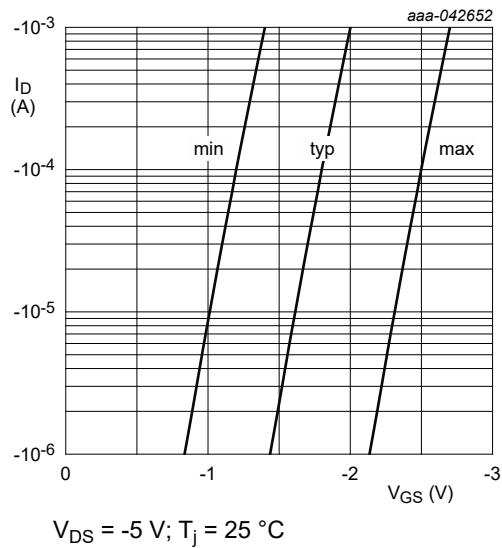


Fig. 6. Sub-threshold drain current as a function of gate-source voltage

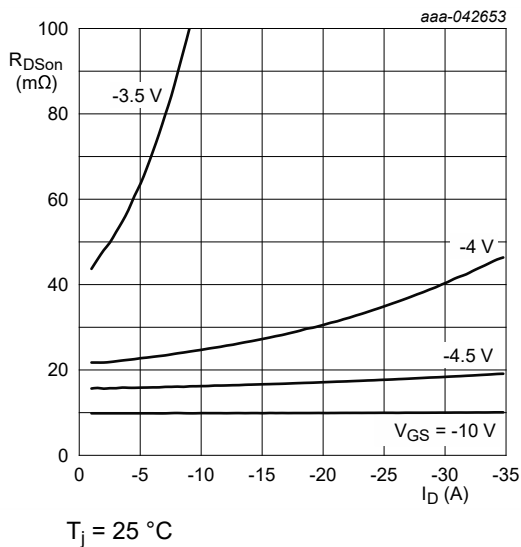


Fig. 7. Drain-source on-state resistance as a function of drain current; typical values

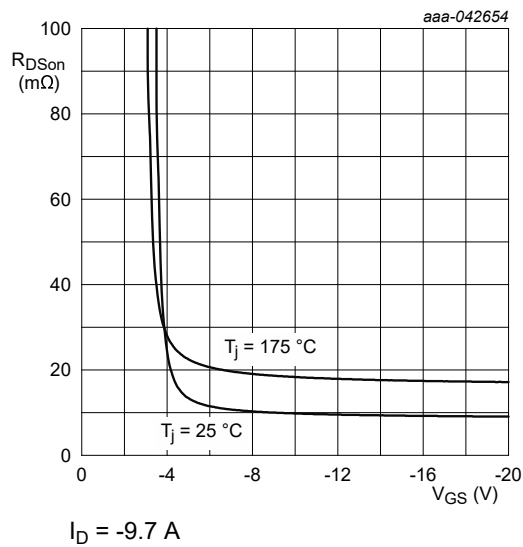


Fig. 8. Drain-source on-state resistance as a function of gate-source voltage; typical values

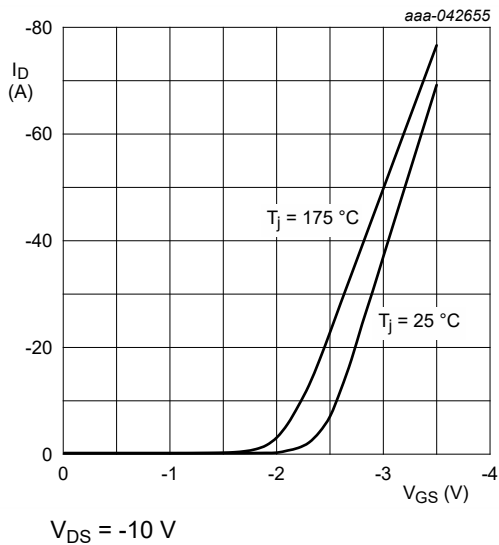


Fig. 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values

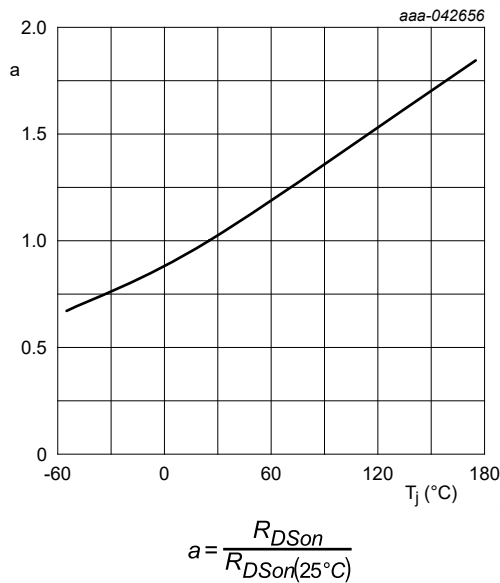


Fig. 10. Normalized drain-source on-state resistance as a function of junction temperature; typical values

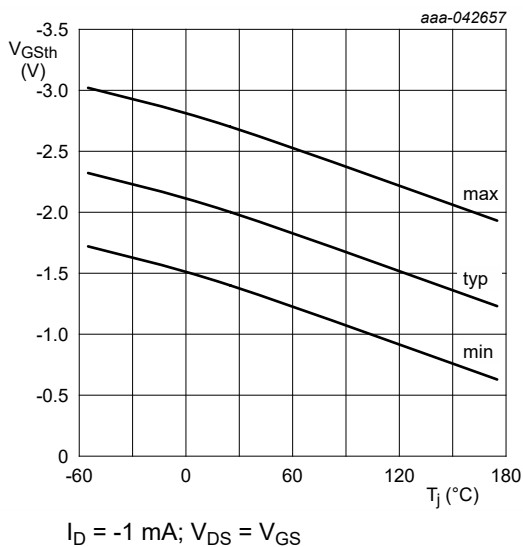


Fig. 11. Gate-source threshold voltage as a function of junction temperature

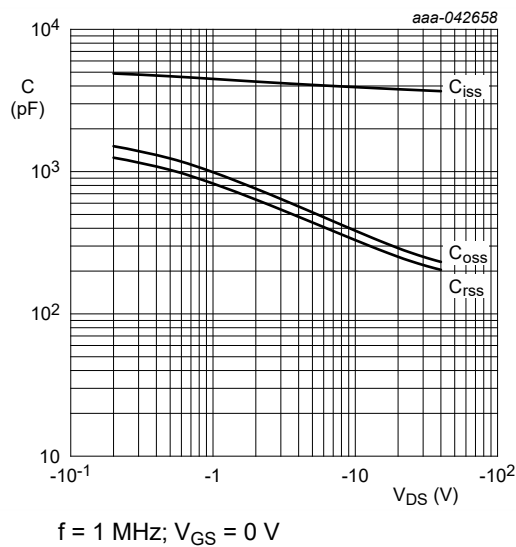


Fig. 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

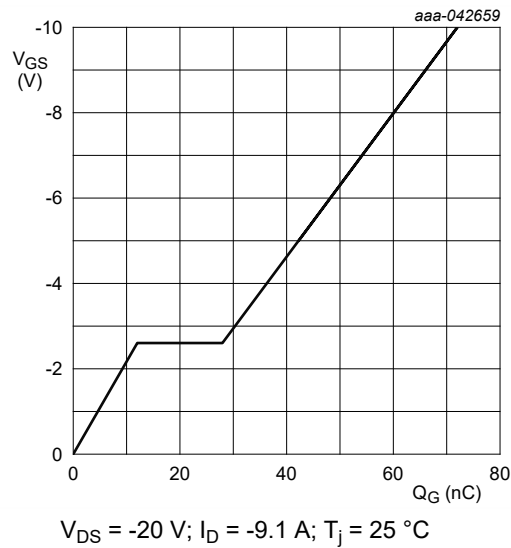


Fig. 13. Gate-source voltage as a function of gate charge; typical values

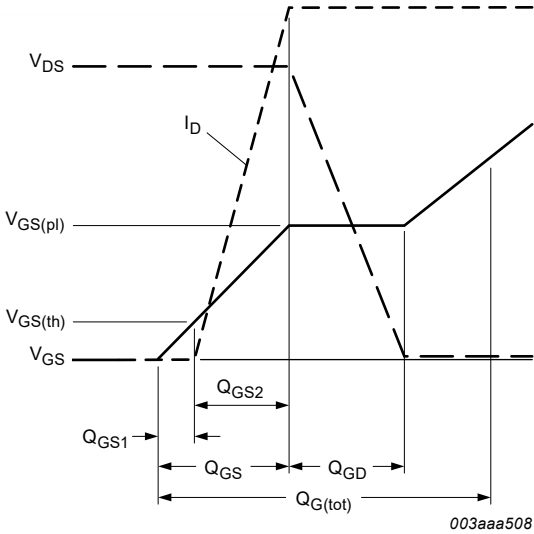


Fig. 14. Gate charge waveform definitions

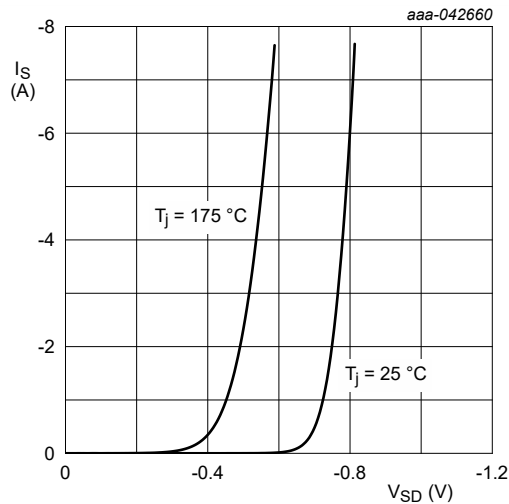


Fig. 15. Source current as a function of source-drain voltage; typical values

11. Test information



Fig. 16. Duty cycle definition

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

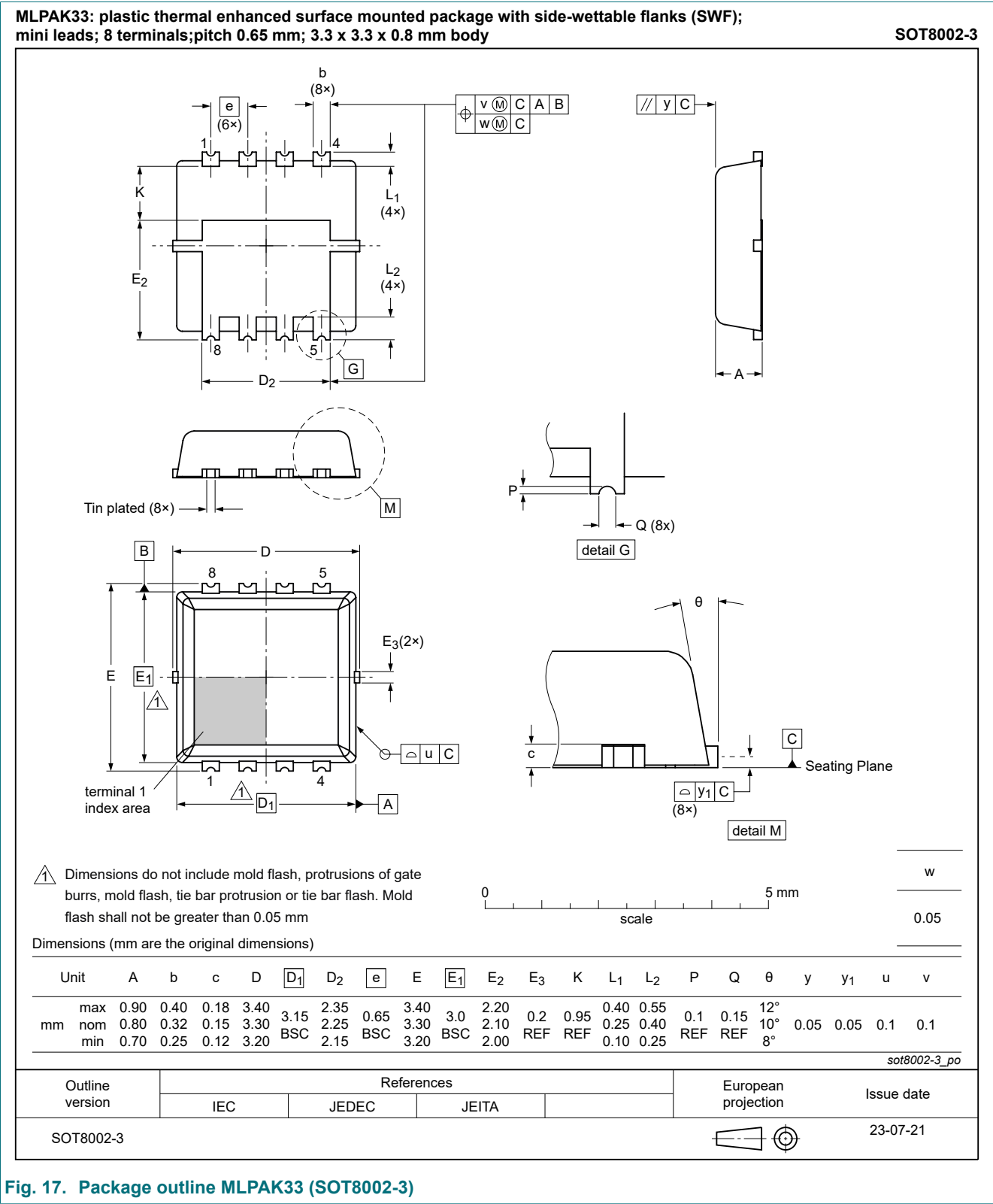


Fig. 17. Package outline MLPAK33 (SOT8002-3)

13. Soldering

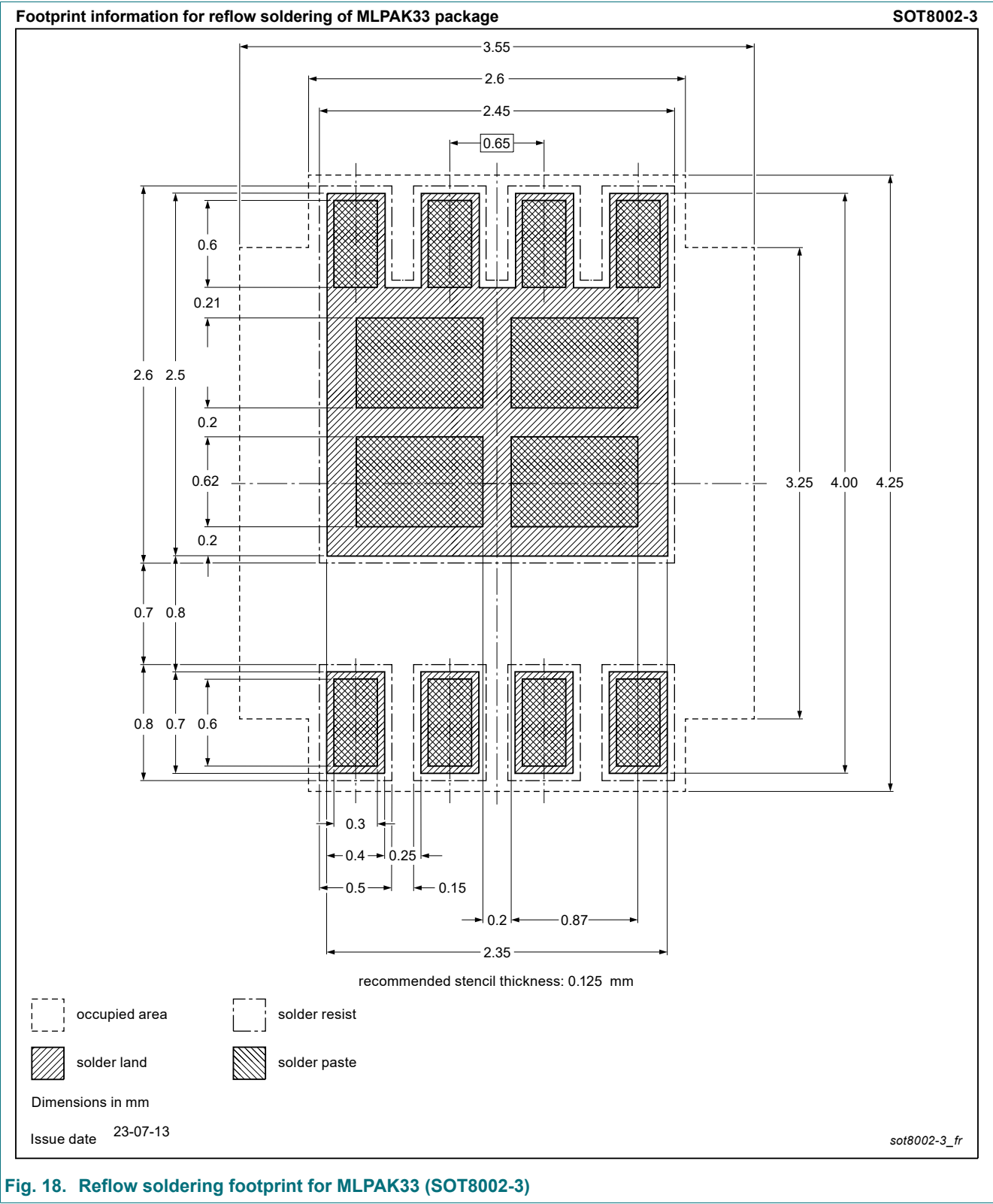


Fig. 18. Reflow soldering footprint for MLPAK33 (SOT8002-3)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
BUK6Q12-40P v.1	20250515	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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